Residual Warnings: 110.

See Table Below for More Details.

**Errors 1-8**: *Synth 8-3917: design EtchaSketch\_TOP has port vga[COLOR][#] driven by constant 0.*

These errors are due to the fact of how we wired the VGA into the FPGA board. As we only output an 8-bit RGB and tied some of the LSBs to 0 as there are ports for 12-bit color, this caused this message. Our wiring here is acceptable and actually preferred as ignoring these ports would be poor form. Furthermore, if these ports are ignored by commenting them out of the Constraints file, then the full RGB colors are never fully realized on the screen, resulting in off-looking coloring.

**Error 9-109**: *Project 1-486: Could not resolve non-primitive black box cell 'BRAM' instantiated as 'mem'[O:/ENGS31/final/final.srcs/sources\_1/imports/sources\_1/imports/new/VGA\_Controller\_top.vhd:225].* And, *Synth 8-3331: design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port [name][#].*

After discussing with Prof. Luke, these errors resulted from the fact that BRAMs have many available features and since we didn’t use them all, they were left unconnected. As we do not need these features and the BRAM runs fine, we determined with Prof. Luke that these errors would not affect performance of our system.

**Errors 110**: *DRC 23-20:* See below for description.

Unresolved: We followed the instructions in the file and added the following lines to the Constraints file. This changed into a Critical Warning, but the design still worked. Therefore we deleted back the following lines from the Constraints file.

set\_property CFGBVS GND [current\_design]

set\_property CONFIG\_VOLTAGE VCCO [current\_design]

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| --- | --- | --- |
| **#** | **Name** | **Details** |
| 1 | Synth 8-3917 | design EtchaSketch\_TOP has port vgaBlue[1] driven by constant 0 |
| 2 | Synth 8-3917 | design EtchaSketch\_TOP has port vgaBlue[0] driven by constant 0 |
| 3 | Synth 8-3917 | design EtchaSketch\_TOP has port vgaGreen[0] driven by constant 0 |
| 4 | Synth 8-3917 | design EtchaSketch\_TOP has port vgaRed[0] driven by constant 0 |
| 5 | Synth 8-3917 | design EtchaSketch\_TOP has port vgaBlue[1] driven by constant 0 |
| 6 | Synth 8-3917 | design EtchaSketch\_TOP has port vgaBlue[0] driven by constant 0 |
| 7 | Synth 8-3917 | design EtchaSketch\_TOP has port vgaGreen[0] driven by constant 0 |
| 8 | Synth 8-3917 | design EtchaSketch\_TOP has port vgaRed[0] driven by constant 0 |
| 9 | Project 1-486 | Could not resolve non-primitive black box cell 'BRAM' instantiated as 'mem' [O:/ENGS31/final/final.srcs/sources\_1/imports/sources\_1/imports/new/VGA\_Controller\_top.vhd:225] |
| 10 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port MUX\_RST[0] |
| 11 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port MEM\_LAT\_RST |
| 12 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port MUX\_REGCE[0] |
| 13 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port WE |
| 14 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port ADDR\_IN[16] |
| 15 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port ADDR\_IN[15] |
| 16 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port ADDR\_IN[14] |
| 17 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port ADDR\_IN[13] |
| 18 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port ADDR\_IN[12] |
| 19 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port ADDR\_IN[11] |
| 20 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port ADDR\_IN[10] |
| 21 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port ADDR\_IN[9] |
| 22 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port ADDR\_IN[8] |
| 23 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port ADDR\_IN[7] |
| 24 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port ADDR\_IN[6] |
| 25 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port ADDR\_IN[5] |
| 26 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port ADDR\_IN[4] |
| 27 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port ADDR\_IN[3] |
| 28 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port ADDR\_IN[2] |
| 29 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port ADDR\_IN[1] |
| 30 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port ADDR\_IN[0] |
| 31 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[63] |
| 32 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[62] |
| 33 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[61] |
| 34 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[60] |
| 35 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[59] |
| 36 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[58] |
| 37 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[57] |
| 38 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[56] |
| 39 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[55] |
| 40 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[54] |
| 41 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[53] |
| 42 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[52] |
| 43 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[51] |
| 44 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[50] |
| 45 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[49] |
| 46 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[48] |
| 47 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[47] |
| 48 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[46] |
| 49 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[45] |
| 50 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[44] |
| 51 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[43] |
| 52 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[42] |
| 53 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[41] |
| 54 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[40] |
| 55 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[39] |
| 56 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[38] |
| 57 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[37] |
| 58 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[36] |
| 59 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[35] |
| 60 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[34] |
| 61 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[33] |
| 62 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[32] |
| 63 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[31] |
| 64 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[30] |
| 65 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[29] |
| 66 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[28] |
| 67 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[27] |
| 68 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[26] |
| 69 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[25] |
| 70 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[24] |
| 71 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[23] |
| 72 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[22] |
| 73 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[21] |
| 74 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[20] |
| 75 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[19] |
| 76 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[18] |
| 77 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[17] |
| 78 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[16] |
| 79 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[15] |
| 80 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[14] |
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| 86 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[8] |
| 87 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[7] |
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| 89 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[5] |
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| 92 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[2] |
| 93 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[1] |
| 94 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port SBITERRIN[0] |
| 95 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port DBITERRIN[63] |
| 96 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port DBITERRIN[62] |
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| 102 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port DBITERRIN[56] |
| 103 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port DBITERRIN[55] |
| 104 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port DBITERRIN[54] |
| 105 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port DBITERRIN[53] |
| 106 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port DBITERRIN[52] |
| 107 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port DBITERRIN[51] |
| 108 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port DBITERRIN[50] |
| 109 | Synth 8-3331 | design blk\_mem\_gen\_mux\_\_parameterized0 has unconnected port DBITERRIN[49] |
| 110 | DRC 23-20 | Rule violation (CFGBVS-1) Missing CFGBVS and CONFIG\_VOLTAGE Design Properties - Neither the CFGBVS nor CONFIG\_VOLTAGE voltage property is set in the current\_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG\_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:   set\_property CFGBVS value1 [current\_design]  #where value1 is either VCCO or GND   set\_property CONFIG\_VOLTAGE value2 [current\_design]  #where value2 is the voltage provided to configuration bank 0  Refer to the device configuration user guide for more information. |